Claims Pending:

1. (Previously Amended) A process for making a semiconductor device comprising the steps of:

performing a LOCOS operation on an epitaxial layer of a semiconductor substrate to define an active region having a predefined boundary;

implanting a first dopant into the epitaxial layer within the active region to create a well of a first type of conductivity;

implanting the first dopant into the well to create a first region and a second region separated from the first region, the first and second regions being implanted across the boundary of the active region and directly spaced apart from each other across the active region and spaced apart from the center of the active region;

depositing a polysilicon layer over the active region;

doping the polysilicon layer to create a poly semiconductor layer of a second type of conductivity;

patterning the poly semiconductor layer to create a poly gate over the first and second regions and well;

performing an ion implant of the second type conductivity between the LOCOS regions and the poly gate to create first and second lightly doped regions, the first and second lightly doped regions being separated by a channel region beneath the poly gate;

depositing an oxide layer over the poly gate and active region;

etching the oxide layer to create side spacers on each side of the poly gate; and

implanting a heavy dose of the second type of dopant between the LOCOS regions and the side spacers to create source and drain regions, the source and drain regions being separated by the first and second lightly doped regions and the channel region.

2. (Original) The process according to claim 1, further including the step of:

implanting the second type of dopant into the semiconductor substrate prior to the step of growing the epitaxial layer.

3.(Original) The process according to claim 2, wherein the first type of dopant is a P type dopant and the second type of dopant is an N type of dopant.

Claims 4-5 (Cancelled)

6. (Previously Amended) The process according to claim 1, wherein the first type of dopant is a P type of dopant and the step of performing an implant of the second type of dopant between the LOCOS regions and the poly gate comprises the step of:

implanting a light dose of N type dopant with each of the first and second lightly doped regions and positioned to be in contact with the first and second regions.

7. (Previously Amended) The process according to claim 1, wherein the step of:

patterning the poly semiconductor layer to create a poly gate includes the step of:

patterning the poly gate over the first and second regions.

8. (Previously Amended) The process according to claim 1, wherein the first type of dopant is a P type of dopant and the step of:

performing an implant of the second type of dopant between the LOCOS regions and the poly gate comprises the step of:

implanting a light dose of N type dopant with each of the first and second lightly doped regions being positioned not to be in contact with the first and second regions.

9. (Original) The process according to claim 1, wherein the step of:

performing an ion implant of the second type conductivity between the LOCOS regions and the poly gate comprises the step of:

implanting a light dose of N type dopant.

10.(Original) The process according to claim 9, wherein the step of implanting a heavy dose of a second type of dopant comprises the step of:

implanting the heavy dose of N type dopant into the first and second lightly doped regions.

11.(Original) The process according to claim 1, wherein the step of:

implanting a heavy dose of the second type of dopant between the LOCOS regions and the side spacers to create source and drain regions, the source and drain regions being separated by the channel region; all included the step of:

patterning the active area using a first reticle to create a pattern on the active region.

12.(Original) The process according to claim 11, wherein the step of:

performing an ion implant of the second type conductivity between the LOCOS regions and the poly gate to create first and second lightly doped regions, the first and second lightly doped regions being separated by a channel region beneath the poly gate included the step of:

patterning the active area using the first reticle to create a pattern on the active region.

13. (Previously Amended) A process for making a semiconductor device comprising the steps of:

performing a LOCOS operation on an epitaxial layer to define an active region;

using a first reticle to create a pattern for implanting a first dopant into the epitaxial layer within the active region to create a well of a first type of conductivity;

using a second reticle to create a pattern for implanting with the first type of dopant into the well to create first and second regions across the boundary of the active region and

spaced apart directly across the active region from each other and spaced apart from the center of the active region;

depositing a polysilicon layer over the active region;

heavily doping with a second dopant the polysilicon layer to create a poly semiconductor layer of a second type of conductivity;

patterning the poly semiconductor layer to create a poly gate;

using a third reticle to create a pattern for lightly doping with a second dopant the active region between the LOCOS regions and the poly gate;

depositing an oxide layer over the poly gate and active region;

etching the oxide layer to create side spacers on each side of the poly gate; and

using the third reticle to create a pattern for heavily doping with the second dopant the active region between the LOCOS regions and the side spacers.

14. (Original) The process according to claim 13, further including the step of:

implanting the second type of dopant into substrate prior to the step of growing the epitaxial layer.

15. (Original) The process according to claim 14, wherein the first type of dopant is a P type dopant and the second type of dopant is an N type of dopant.

16. (Cancelled)

17. (Previously Amended) The process according to claim 13, wherein the first type of dopant is a P type of dopant and the step of lightly doping the second type of dopant between the LOCOS regions and the poly gate comprises the step of:

implanting a light dose of N type dopant wherein each of the first and second lightly doped regions are in contact with the first and second regions.

18.(Original) The process according to claim 17, wherein the step of heavily doping with the second dopant comprises the step of:

implanting the heavy dose of N type dopant into the first and second lightly doped regions.

19. (Original) The process according to claim 18, wherein the step of patterning the poly semiconductor layer to create a poly gate includes the step of:

patterning the poly gate over the first and second regions.

20. (Original) The process according to claim 13, wherein the step of:

using the first reticle to create a pattern for lightly doping with the second dopant the active region between the LOCOS regions and the poly gate comprises the step of:

implanting a light dose of N type dopant.

21.(Original) The process according to claim 20, wherein the step of:

using the first reticle to create a pattern for heavily doping between the LOCOS regions and the poly gate comprises the step of:

implanting a heavy dose of N type dopant.